Effects of Package Level Structure and Material Properties on Solder Joint Reliability Under Impact Loading

Xuejun Fan, Amarinder Singh Ranouta, and Harpreet Singh Dhiman

***Abstract*— In this paper, the effects of package level structures and material properties on solder joint reliability subjected to impact loading are investigated by the integrated experimental testing, failure analysis, and finite element modeling. Three different package structures: ball on I/O wafer level package (WLP), copper post WLP, and chip-scale (CS) ball grid array (BGA) package, are studied. Experimental testing based on JESD22-B111 is conducted to obtain the components' failure mode, rate, location, and the corresponding board strains and accelerations. Finite element models are developed and validated against the experimental results. For a CS BGA package, the compliance of the plastic substrate/mold compound provides a "stress buffer mechanism" at corner joints in BGA to relieve stresses. For a copper post (or pillar) WLP, wafer level epoxy, which encapsulates copper pillars, serves as a compliant layer for solder joint stress reduction under dynamic loading. Comprehensive data from simulation and experimental results show that package structure and material properties play a significant role on the dynamic responses of solder joints. The actual solder joint reliability performance of a CS BGA or WLP package depends on the resultant effects of package structure, material properties, package body size, and the component locations.**

***Index Terms*— Ball grid array (BGA), compliant layer, dynamics, finite element analysis (FEA), impact loading, JESD22-B111, reliability, solder joints, wafer level package (WLP).**

I. Introduction

CHIP SCALE (CS) ball grid array (BGA) and wafer level packages (WLP) are two major packaging options for low pin count electronic devices in handheld applications. CS BGA packages, which usually apply for wire-bond devices, are defined for the package/die size ratio less than 1.2. Conventional (fan-in) WLPs [1], on the other hand, are a unique form of packages and have the distinction of being truly die-sized, not "CS." They are formed on the dies while they are still on the uncut wafer. There have been a variety of WLP technologies with distinct package structures. Standard ball on I/O WLP has evolved with the incorporation of redistribution layer (RDL) process, copper post process, and compliant layer process [2], [3].

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A mechanical impact resulting from mishandling, such as being dropped during transportation or customer usage, may cause solder joint failures of these packages. A board level drop test method, JESD22-B111 [4], has been standardized to evaluate the performance of integrated circuit packages under standard drop conditions. Three primary failure modes are often observed in drop test for BGA and WLP packages: copper trace crack or pad crater in printed circuit board (PCB), crack at intermetallic (IMC) layer of solder joints, and die-level cracks, such as in RDL or copper interconnect. Because PCB failures (trace crack or pad crater) provide a misrepresentation of the actual package performance, some board design guidelines have been further recommended and adopted to avoid such failure modes during test [5].

To correlate board level dynamic responses to component failures, a multichannel real-time monitoring system has been applied to obtain board strains and accelerations at various locations of PCB using strain gages and accelerometers [6], [7]. A digital image correlation system integrated with the high speed cameras has also been developed to acquire the images of entire surfaces of dynamic deformation of board [7]. Various shock/impact modeling techniques have been developed to predict board dynamic strains and transient solder joint stresses. Explicit dynamics has been applied in both product and board levels [8]–[10]. The so-called input-G method has been widely adopted since it decouples the board finite element model from the system model [11]. There are several approaches in implementing the input-G method, such as explicit dynamics analysis using DYNA-3-D [12], large mass method with implicit dynamics [13], and the input-D method, in which the acceleration input is integrated twice to obtain the displacement boundary condition over time [14]. Mode superposition method is also applied effectively for a linear system under impact loading [15]. Shen and the authors introduced the direct acceleration input method as an alternative to apply the impulse loading while removing the rigid body motion. In this method, the acceleration impulse is applied as body forces to the problem under study [16]–[20]. There are a number of special numerical treatments developed in finite element models to reduce the problem sizes, such as equivalent layer model for solder interconnects [17], shell element application in global models [13], shell-to-solid sub-modeling using beam-shell-based elements [21], [22]. The accuracy of the local modeling (or sub-modeling) technique has been verified by the comparison of board strain calculations from both global and local models [17].

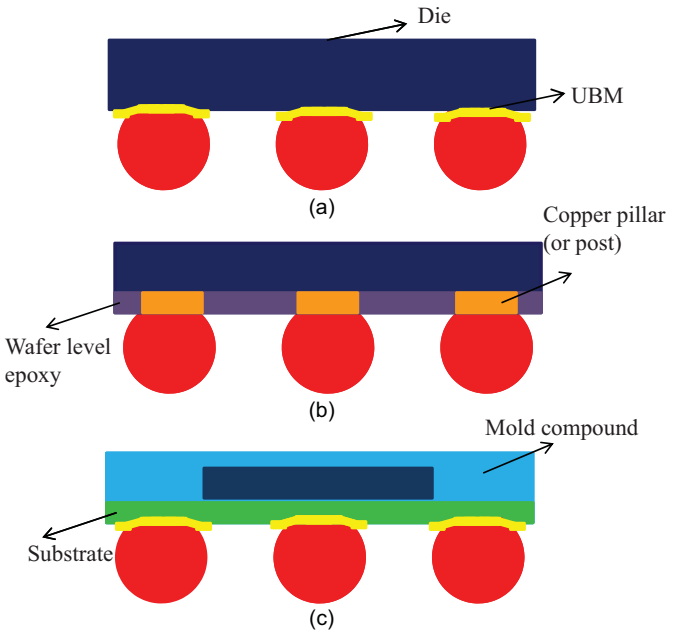


Fig. 1. Illustrations of package structures (not drawn to scale): (a) ball on I/O WLP, (b) copper post WLP, and (c) CS BGA package.

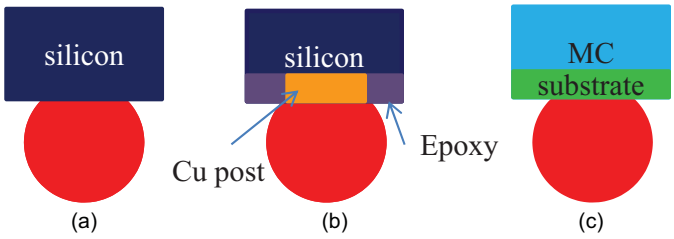


Fig. 2. Materials and structures at package corner. (a) Ball on I/O WLP. (b) Copper post WLP. (c) BGA package. (Solder pad and UBM layer are omitted for clarity.)

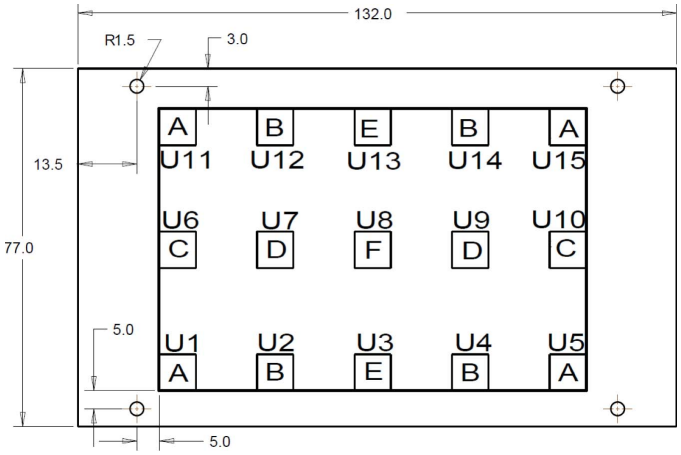


Fig. 3. JESD22-B111 drop test board configurations and component placements.

Numerous experimental and test data have been reported for solder joint reliability under impact loading on BGA packages and WLPs [5], [13], [23]. However, little study has been conducted across an array of various package structures for solder joint reliability under impact loading. This is probably due to the fact that there are so many variations in geometries and materials that it is difficult to have a single straightforward comparison [24]. Moreover, there has been a lack of systematic approach to understand the contributing factors to solder joint drop reliability for these packages.

In this paper, integrated experimental analysis, failure analysis, and finite element modeling are performed to investigate the mechanisms of reliability performance for various CS BGA and WLPs. Three package structures under study are described in the next section. Experimental setup, failure analysis, and test results are discussed in Section III. Section IV introduces the mathematical formulations and finite element models, and Section V gives the experimental validations. The detailed results and discussions are presented in Section VI, with concluding remarks in Section VII.

II. Package Structures

Three package structures are studied in this paper: ball on I/O WLP, copper post WLP, and CS BGA, as shown in Fig. 1. Ball on I/O WLP is a standard wafer level packaging format, which is similar to a typical flip chip structure. In this configuration [Fig. 1(a)], balls are attached to the aluminum pad directly through under bump metallurgy (UBM). While the ball on I/O WLP is no longer a viable technology in WLP production due to poor fatigue performance [2], it is used as a benchmark case for comparison analysis. In a copper post WLP structure [Fig. 1(b)], thick copper pillars (e.g., ~70-μm thickness) are electroplated, followed by an epoxy encapsulation at wafer level. The third case is a typical CS BGA package, as shown in Fig. 1(c).

Previous studies have shown that the corner solder joints are most vulnerable under mechanical impact [5], [13], [20], [23]. Thus, in this paper, we will focus on the transient responses of the corner joints in each package. Fig. 2 depicts the schematic view of the structures of corner joints in the three packages. In ball on I/O WLP [Fig. 2(a)], the corner solder ball is attached to the silicon die directly. The UBM layer is omitted for clarity. Fig. 2(b) shows a copper post WLP structure, in which a copper/epoxy layer is placed between silicon die and ball. For a BGA package, corner ball is attached to the substrate/mold compound (the pad and UBM layer are omitted).

III. Experimental Setup and Test Results

According to JESD22-B111, a 132 × 77 × 1 mm eight-layer PCB is used for the drop test. Fifteen components are mounted on the board in three rows of five components, as illustrated in Fig. 3. Based on the symmetry, the 15 components are classified into five groups from A to F. The JEDEC test board is mounted on a base plate with four screws at the corners. The base plate is then mounted on a drop table. The drop table, guided by guide rods, is allowed to strike on a rigid base from some specified height H. The Lansmont model 65/81 drop impact tester was used to carry out the board level drop impact test. A half sine impulse is produced when the table strikes the rigid base. Condition B in JESD22-B111 is used for this paper. The input acceleration to the board has

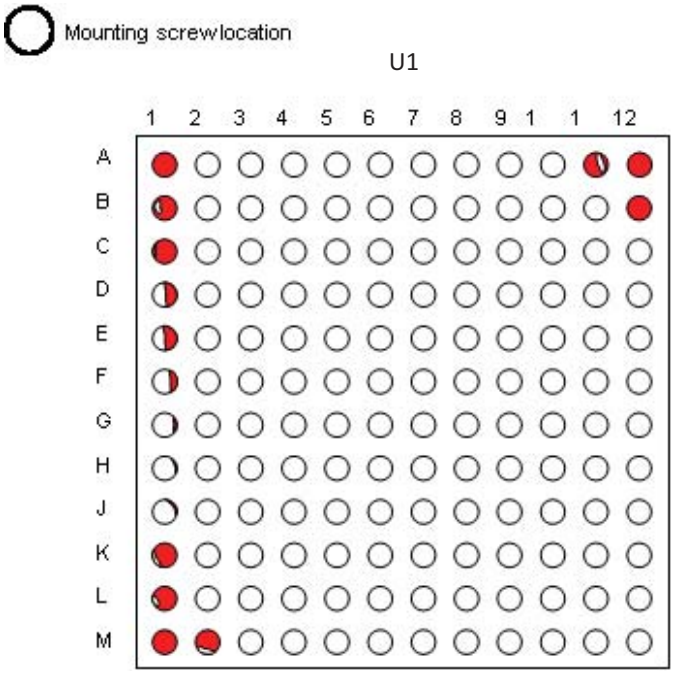


Fig. 4. Crack map of group A WLP after drop test (red areas correspond to solder joint IMC crack at package side).

1500-g peak and 0.5-ms duration, which can be described by equation as follows:

$$a = \begin{cases} 1500g \sin\frac{\pi t}{t_w}, & t \le t_w, t_w = 0.5 \\ 0, & t \ge t_w \end{cases} \quad (1)$$

where a is the acceleration of the drop table, g is acceleration due to gravity (9.8 m/s^2), and t_w is the impulse duration (ms).

Strain gauge rosettes are used to measure board strain transient responses at various locations. The comparison between the strain measurement and finite element results will be discussed in Section V. Dye and pry techniques are applied for failure analysis for the selected components to determine the failure mode and crack propagation pattern. The dominant failure mode in this study was the solder joint crack at IMC layer on the component side. A typical failure map showing crack size and locations is illustrated in Fig. 4. It is seen that the solder joints at left and right columns show the most crack propagations compared to the other columns. In addition, the cracks initiate from solder joint inner side and propagate toward opposite side.

A typical Weibull plot for the failure rate of all six groups is shown in Fig. 5 for a 6 × 6 mm WLP package. A total of ten test boards were tested to have sufficient failure data points for all groups. For the package size of 6 × 6 mm, the failure rate rank is: A>F>E>B>D>C. It is seen that group A (corner components) has the greatest failure rate, followed by groups F and E (center row components). Groups B, C, and D have the smallest failure rates.

For various types of packages with various sizes, it is generally seen that the first resonant frequency of the test board is registered around 230 Hz, and the second one is found at approximately 650 Hz.

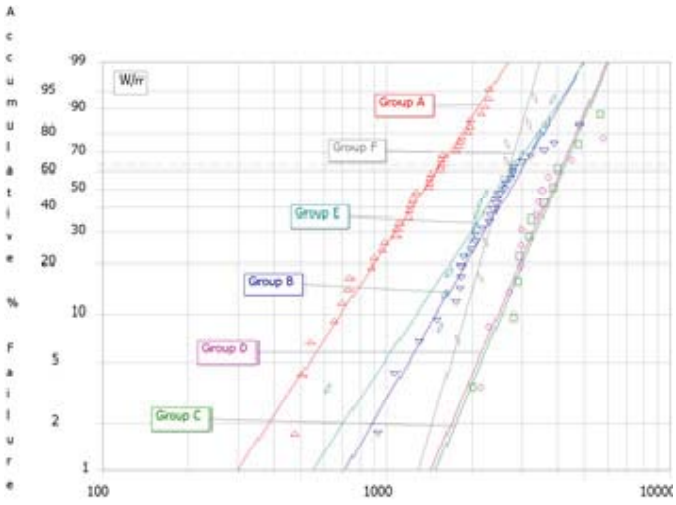
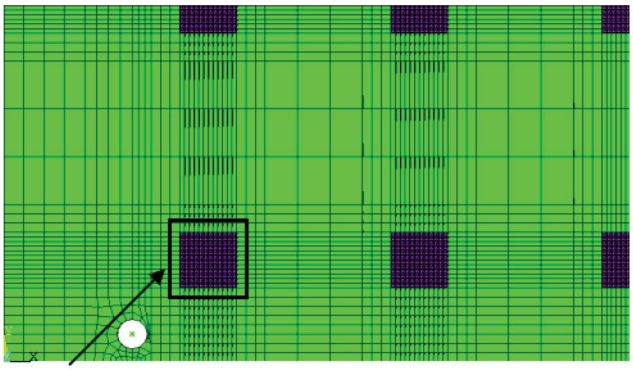
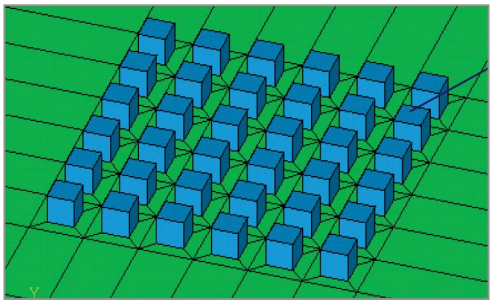


Fig. 5. Weibull plot of drop test failures for six component groups for a 6 × 6 mm copper post WLP.



(a)



(b)

Fig. 6. Quarter global finite element model. (a) Global finite element model for board and (b) solder joint finite element mesh in global model.

IV. Mathematical Formulations and Finite Element Models

For JESD22-B111 drop test, the main interest is the component dynamic responses, especially the solder joint transient stresses. In solving a dynamic problem, it is important to know whether the problem falls into the category of wave propagation or structural transient dynamic response. It may be

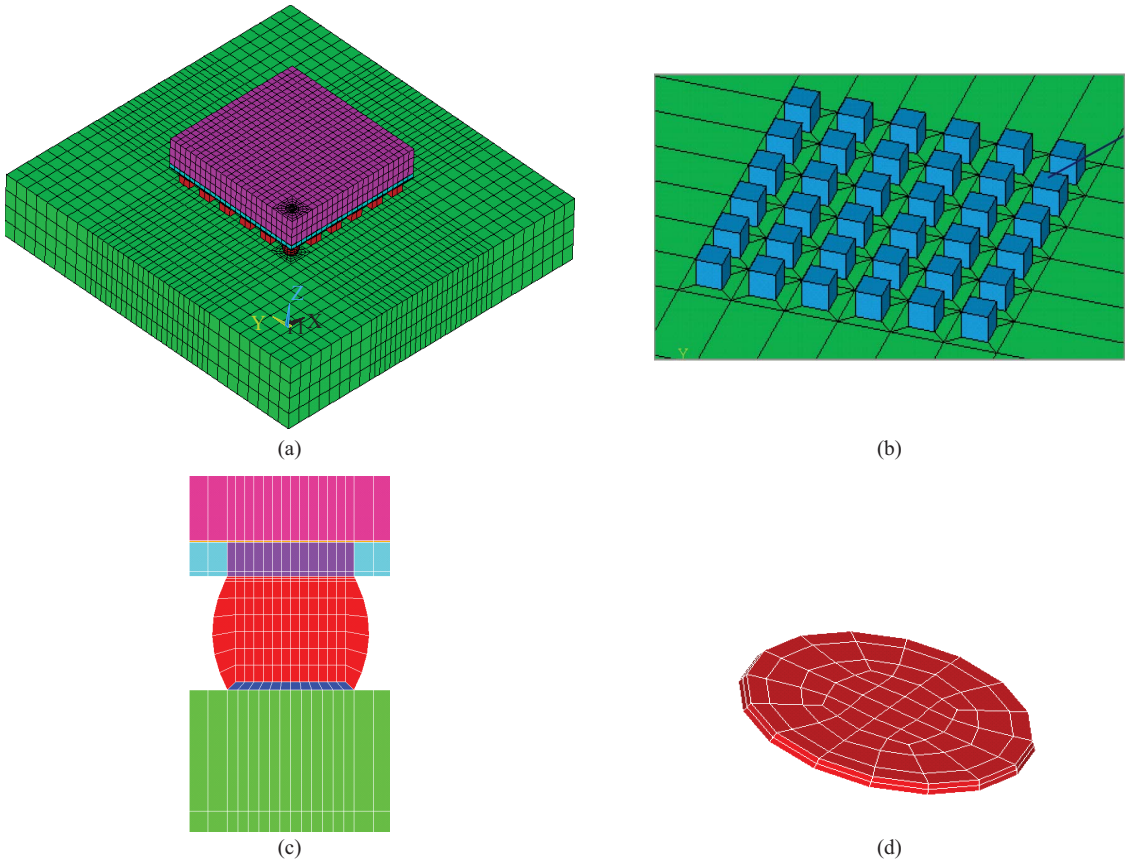


Fig. 7. Local finite element model. (a) Overall local model. (b) Details of solder joint finite element model. (c) Cross-section of refined meshes of corner joints. (d) IMC layer finite element mesh.

helpful to compare the time scale of stress wave propagation in PCB to a typical impulse scale (0.5 ms per JEDEC definition) and PCB dimension. The speed of stress wave is $\sqrt{\mu/\rho}$, where μ and ρ are shear modulus and density of the board. The value is approximately 7×10^3 mm/ms, which means that the stress wave has already traveled back and forth in PCB (~130-mm length) several times within 0.5 ms to reach an equilibrium of being bulk structural dynamic responses. Therefore, the problem under study is solved by structural dynamics.

For the loading condition described in (1), the load in terms of acceleration on mounting screws can be converted to body forces of board (so-called direct acceleration method), with the formulation as follows:

$$\{M\}[\ddot{u}] + \{C\}[\dot{u}]\{K\}[u] = \begin{cases} -\{M\}1500g \sin\frac{\pi t}{t_w} & t \le t_w, t_w = 0.5 \\ 0 & t \ge t_w \end{cases} \quad (2)$$

and initial conditions

$$[u]|_{t=0} =, \qquad [\dot{u}]|_{t=0} = \sqrt{2\mathrm{gH}} \quad (3)$$

where H is the specified drop height, $[M]$ the mass matrix of the system, $[\dot{u}]$ is the acceleration, $\{C\}$ is the damping matrix, $[\dot{u}]$ is the velocity vector, $\{u\}$ is the stiffness matrix, g is acceleration due to gravity, $[u]$ is the displacement, and t is time after impact. If no-rebound of the drop table takes place, the following boundary conditions apply for the board:

$$[u]|_{\text{at monting location}} = 0. \quad (4)$$

The above equations have been proved analytically to be equivalent to the original problem formulations, and are also verified numerically by the finite element analysis (FEA) [17].

Global and local finite element modeling approach is used, as shown in Figs. 6 and 7. In the global finite element model, a quarter JEDEC board is modeled due to symmetry conditions. Coarse meshes are applied, and solder joints are simplified as rectangular blocks. A local finite element model contains one component, with an extended PCB board dimension (cut boundary is 2 mm away from the component edge in both x and y directions). Fig. 7 shows an example of a local model for component U1. In the local model, the critical (corner) solder joint(s) include all details of material and geometry with refined meshes. Since the primary failure is at the intermetallic layer on the component side, a 10-μm layer with two layers of elements is created at the critical solder joint upper interface.

It is worthy to note that the symmetry conditions are applied in above finite element models. It is known that both symmetric and anti-symmetric dynamic modes exist in such a system in a dynamic analysis. The half- or quarter-finite element model will eliminate anti-symmetric vibrational modes. However, since the both structure geometry and loading conditions are symmetric, the anti-symmetric modes are never excited.

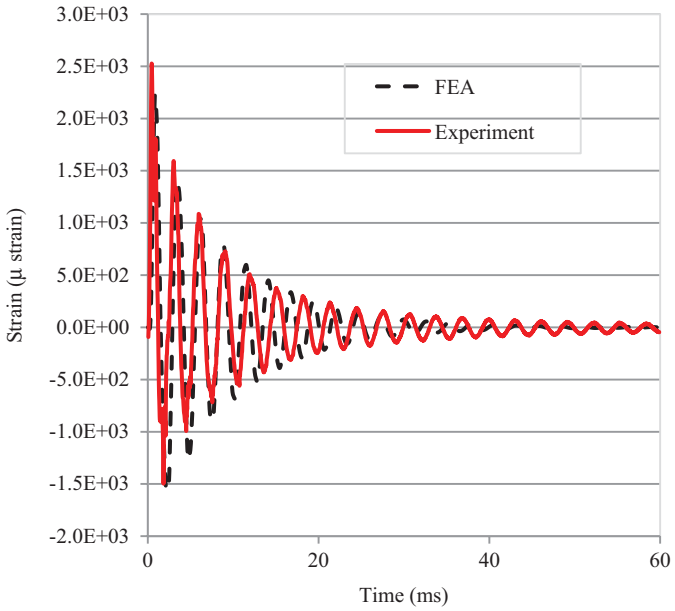


Fig. 8. Comparison of bare board strain history.

Inclusion of the anti-symmetric modes does not make a difference if symmetric load is applied. Our study has verified that the same results can be obtained [17] for a full model, half-model, and quarter model, with the symmetric load applied. Therefore, in this paper, a quarter JEDEC board is used in order to reduce model size and solution time. Implicit dynamics, which is available for most of the standard commercial finite element software, is applied to solve the above problems.

V. Experimental Validations

The damping coefficient of the PCB used in the FEA is calibrated through board strain history measurement. Bare board without components is tested for this purpose. Fig. 8 shows the overall comparison of entire strain history during impact, with a damping coefficient of 0.07. The damping coefficient is then used to predict the board strains at component corners at various locations. Fig. 9 plots a typical strain time history comparison in the first period of board vibration for the components U11 and U8 in x-direction, respectively. FEA predicts the board strain dynamic responses very well.

Modal analysis is also performed with the global finite element model. The first two symmetrical modes and the corresponding fundamental frequencies are calculated as 220 and 654 Hz, respectively, from modeling. Modeling results correlate very well with measured data 230 and 650 Hz.

Fig. 10 shows the top view of peeling stress contour of all solder joints for the corner component U1 from the global FEA. The results explain well the crack propagation map shown in Fig. 4. The detailed stress contour at the corner solder joint from local finite element model is shown in Fig. 11. It confirms that the cracks initiate from solder joint inner side and propagate toward opposite side.

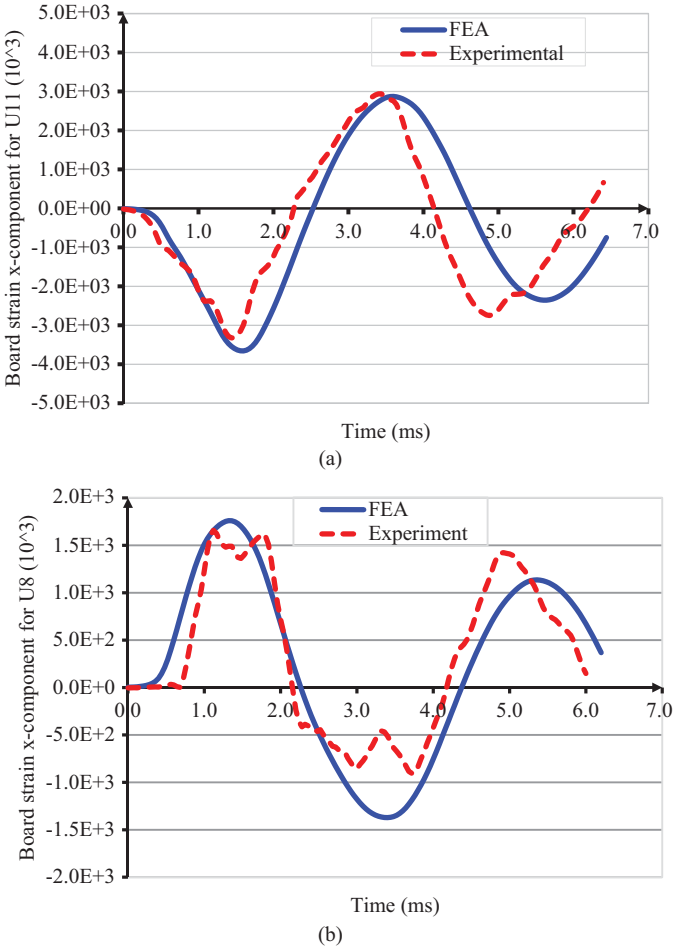


Fig. 9. Comparison of finite element results with experimental measurements (a) ε_x for U11 and (b) ε_x for U8.

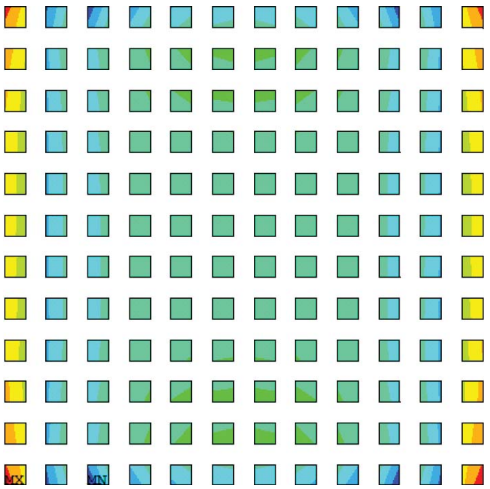


Fig. 10. Tensile stress contour at U1 from global finite element modeling.

VI. Modeling Results and Discussion

A. Effect of Package Body Size and Location

The WLP package with the array size from 6 × 6 to 28 × 28 on a ball pitch of 0.5 mm (i.e., package body size ranges from 3 × 3 mm to 14 × 14 mm) is studied. Fig. 12 shows the maximum peeling stress at components U1, U3, and U8,

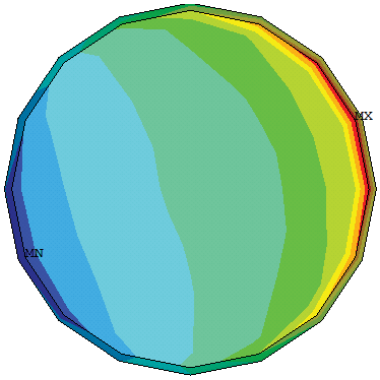


Fig. 11. IMC tensile stress contour from local FEA for corner joint of U1 component.

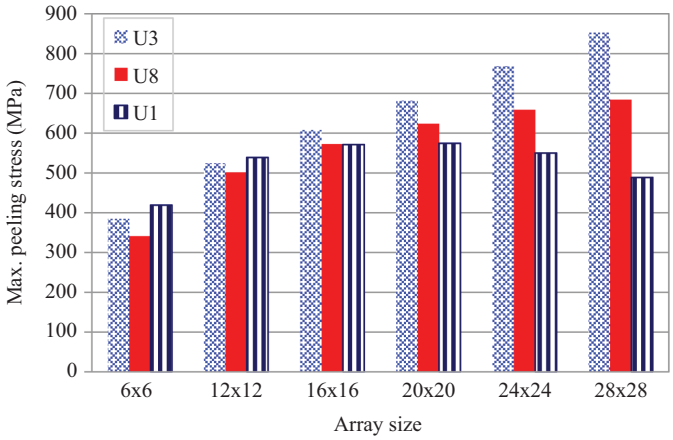


Fig. 12. Maximum peeling stresses for different array sizes of copper post WLP package of U1, U3, and U8.

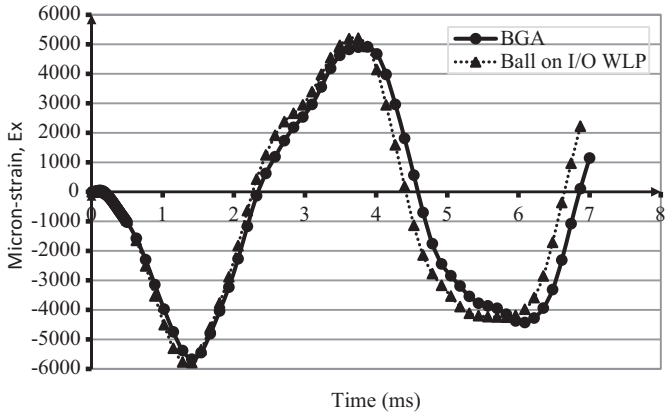


Fig. 13. x-direction PCB strain at the corner of U1.

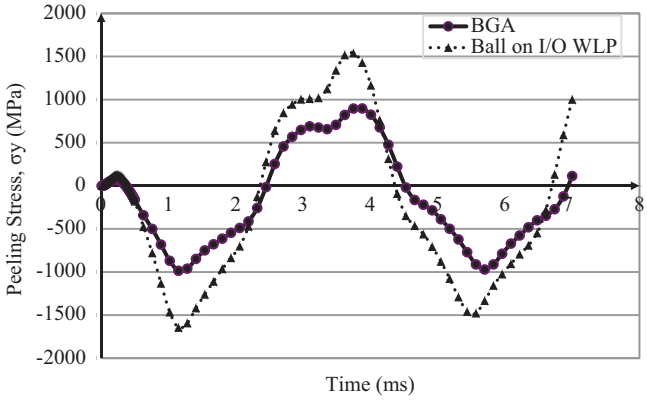


Fig. 14. Peeling stress history of the corner solder joint in U1.

respectively. When the package size is 6 × 6 mm, the failure rate rank for these three groups is A(U1)>F(U8)>E(U3), which is consistent with the experimental data shown in the Weibull plot in Fig. 5. However, when the package size is 20 × 20 mm, the rank becomes E(U3)>F(U8)>A(U1). This suggests that U1 component (or group A) would fail first when the package size is less than 10 × 10 mm, but the central components U3 or U8 would fail earlier than U1 for a larger component. These have been verified experimentally. From Fig. 12, it is seen that the solder joint stresses for U3 and U8 increase monotonically when package size increases. However, for the corner component, the relationship between the solder joint stress and package size is not monotonic. The solder joint stress increases from 6 × 6 to 16 × 16 array, and decreases from 20 × 20 to 28 × 28 array.

B. Comparison Between Ball on I/O WLP and CS BGA Package

It is of interest to understand how different package structures can lead to different drop performance. Ball on I/O WLP and CS BGA packages are compared first. Assume that both packages have 0.5-mm ball pitch and the array size of 12 × 12. Fig. 13 plots the board strain as a function of time during drop for two packages, respectively. It is seen that the PCB board strains are approximately the same. Evidently the package structure has little effect on the global PCB dynamic responses, as their body sizes are the same. However, the magnitudes of solder joint stresses are significantly different for these two packages, as shown in Fig. 14. The peak tensile stress in CS BGA package is 44% less than in the ball on I/O WLP (see Table I). The discussion on the difference will be given in the next section.

TABLE I
PEAK TENSILE STRESSES AT CORNER SOLDER JOINTS IN BALL ON I/O WLP AND CS BGA PACKAGES

	Ball on I/O WLP Package	CS BGA Package
Peak tensile stress in the corner solder joint (MPa)	8.62×10^2	1.54×10^3

PCB strain measurement at package corners is usually considered as a metric to evaluate the stress level in solder joints under impact loading. The argument is that the solder joints are stressed mainly due to board bending, and PCB strain is a parameter that can be measured directly in assembly and test. The above results suggest that solder joint stresses depend not only on the PCB bending, but also on the package structure and materials adjacent to the joints (local effect).

TABLE II
MAXIMUM PEELING STRESSES AND BOARD STRAINS FOR COPPER POST WLP AND BALL ON I/O WLP*

Package Type	Copper Post WLP				Ball on I/O WLP	CS BGA
Epoxy modulus (GPa)	4.7	14	20	130	N/A	N/A
Max peeling stress (MPa)	**5.39×10^2**	8.22×10^2	9.43×10^2	1.61×10^3	**1.54×10^3**	**8.62×10^2**
Max board strain (10^{-6})	4.63×10^3	4.67×10^3	4.69×10^3	4.77×10^3	5.67×10^3	4.87×10^3

*The stress data are for U1, and strain data are at board near U1 corner per IPC specification.

C. Copper Post WLP Package

In a copper post WLP, there is an epoxy/copper post layer between solder ball and silicon (Fig. 1). The modulus of the wafer level epoxy may vary, typically, ranging from 4–20 GPa [2]. Thus, a parametric study is performed to understand the effect of epoxy modulus. Table II shows the results of board strains and maximum peeling stresses for different values of epoxy modulus. The results are also compared to a ball on I/O WLP, and a CS BGA package. It is seen that solder joint stresses decrease dramatically with the decreasing of epoxy modulus. As an extreme case, when the epoxy modulus approaches 130 GPa, which is the modulus of silicon, the solder joint stress in the copper post WLP is almost the same as the stress in ball on I/O WLP. Since the epoxy used in copper post WLP is only a fraction of the modulus of silicon die, the stress in a copper post WLP is significantly lower than the stresses in ball on I/O WLP. Also, as expected, it is seen from Table II that the board strain stays almost the same while joint stress changes with different epoxy modulus.

Why are the stresses in solder joints very different among these three packages? What are the mechanisms behind the results shown in Tables I and II? Fig. 15 attempts to explain the mechanisms of the solder joint stress reduction in CS BGA and copper post WLP packages. In a CS BGA package, the corner joints are attached to the plastic substrate/mold compound, which may be viewed as a spring network in both vertical and horizontal directions, as illustrated in Fig. 15(b). This is in contrast with the ball on I/O WLP package [Fig. 15(a)], in which the solder joints are attached to a rigid silicon die directly. The compliance of substrate and mold compound in a BGA package can relieve the solder joint stresses significantly during impact. From Table I, it can be seen that the stress is reduced by almost 44% compared to a ball on I/O WLP package.

On the other hand, for a copper post WLP package, wafer level epoxy may act as a horizontal spring, as illustrated in Fig. 15(c). Since the epoxy is very compliant compared to the silicon, the stresses in solder joints can be reduced greatly, depending on the modulus of epoxy. When the modulus is about 4.7 GPa, the stress in solder joint is reduced by 70% compared to a ball on I/O WLP (Table II).

It was known that the epoxy layer in a copper post WLP package serves as a stress buffer layer during thermal cycling to improve the solder joint fatigue performance greatly [2]. From the above analysis, it appears that such a compliant layer also provides a "buffer" effect for solder joints under impact loading. Ideally, the more compliant of the buffer layer is, the less the stresses in solder joints. But new failure mode may appear: epoxy crack and RDL (embedded in the epoxy layer)

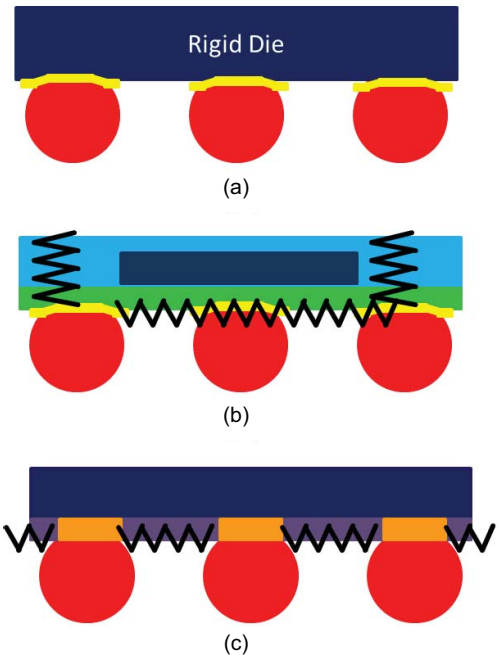


Fig. 15. Illustrations of stress reduction mechanisms. (a) Benchmark case: a standard WLP. (b) Spring network due to the compliance of plastic substrate and mold compound in a BGA package. (c) Horizontal "springs" due to the compliance of wafer level epoxy layer.

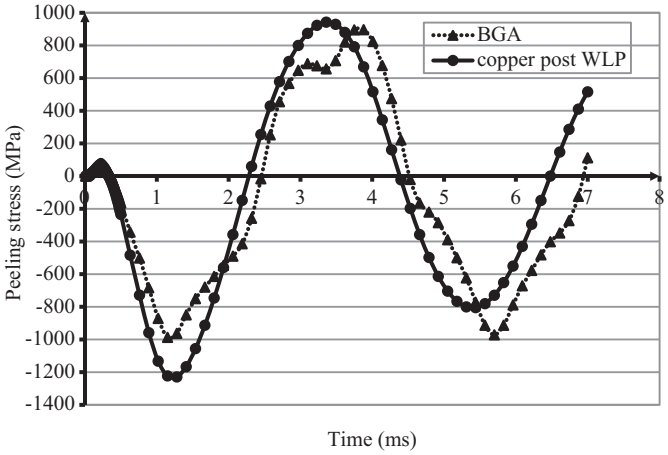


Fig. 16. Peeling stress history of BGA versus copper post WLP (epoxy modulus = 20 GPa).

failure. A tradeoff design must be considered in the selection of compliant layer material, such as wafer level epoxy in copper post WLP.

D. Resultant Effects

To compare solder joint performance in a BGA package versus a copper post WLP package, there are three major contributing factors: package body size, epoxy modulus, and thickness (for copper post WLP), and substrate and mold compound properties and geometry (for BGA), given that solder joints are the same. As an example, if a same device (die size) is packaged with both BGA and copper post WLP, which means that the BGA body size will be larger than WLP, Fig. 16 plots the resultant peeling stress history of the BGA and copper post WLP. It is seen that the stress levels for both packages are approximately the same for the given material sets (wafer level epoxy modulus is 20 GPa). Experimental data show that, statistically, there is no significant difference in terms of failure rate for this case study.

VII. Conclusion

This paper presented an integrated study of experimental testing, failure analysis, and finite element modeling to investigate the effects of structures and material properties at package level on solder joint reliability under impact loading. The main findings and conclusions are summarized as follows.

1) Board strain history, fundamental frequency, and failure maps obtained from experiments are used to validate the finite element modeling predictions. The quarter finite element model is sufficient since both geometry and the load are symmetric. The dynamics of JESD22-B111 test board is described by structural dynamics (not wave propagation) due to the time scale considered.
2) The dominant failure observed in this paper is the crack in the IMC layer at corner solder joints on the component side. The crack initiates from the inner side of the solder joints and propagates outward, which are also verified by the FEA.
3) Peeling stress of the components in the center row (groups U3 and U8) increases monotonically when package size increases. However, the solder joint stress decreases with increasing package size for the corner components (U1), when the package size is greater than 10×10 mm. Because of this, the experimental results have shown that, for larger packages, the components located in the center rows fail first. However, the failure of the components at corners occurs early in the smaller packages. The finite element modeling results align well with the experimental observations.
4) For a CS BGA package, it is found that corner solder joint solder stress is significantly less (about 44%) than that in a ball on I/O WLP. Plastic substrate and mold compound provides a damping effect for the reduction of solder joint stress.
5) For a copper post WLP package, the wafer level epoxy, which is used to encapsulate copper pillars, acts as a horizontal spring structure to relieve the stress during impact. It appears that the epoxy layer serves as a stress buffer layer in WLP to relieve the stress during impact.
6) For a comparison of drop performance between WLP and CS BGA packages, there may be several major contributing factors, including: package body size, epoxy modulus, and thickness (for copper post WLP), and substrate and mold compound properties and geometry (for BGA), given that solder joint conditions are the same. Overall, the smaller size of the package, along with the compliant structure between the solder joints and die, will improve the package drop reliability under impact loading.

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